

a first signal path for guiding a test input signal, which has been supplied to a first pad, to a signal input terminal of said circuit block;

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a second signal path for guiding a test clock, which has been supplied to a second pad, to a clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad; and

a fourth signal path for guiding said test clock, which is input to said clock input terminal, to a fourth pad,

wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal.

22. The semiconductor device according to claim 21, wherein said first signal path comprises a selector which during a normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during a test operation supplies said test input signal to said signal input terminal of said circuit block.

23. The semiconductor device according to claim 21, wherein said second signal path comprises a selector which during a normal operation supplies a normal

clock to said clock input terminal of said circuit block, and which during a test operation supplies said test clock to said clock input terminal of said circuit block.

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24. The semiconductor device according to claim 21, wherein said third signal path comprises a selector which during a normal operation supplies a prescribed signal other than said test output signal to said third pad, and which during a test operation supplies said test output signal to said third pad.

25. The semiconductor device according to claim 21, wherein said fourth signal path comprises a selector which during a normal operation supplies a prescribed signal other than said test clock to said fourth pad, and which during a test operation supplies said test clock to said fourth pad.

26. A semiconductor device having an access time measuring test mode, comprising:

a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;

a first signal path for guiding a test input signal, which has been supplied to a first pad, to a signal input terminal of said circuit block;

a second signal path for guiding a test clock, which has been supplied to a second pad, to a clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block;

a fourth signal path for guiding said test clock, which is input to said clock input terminal; and

a selector which selectively supplies said test output signal from said third signal path or said test clock from said fourth signal path to a third pad.

27. The semiconductor device according to claim 26, wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth paths are substantially equal.

28. The semiconductor device according to claim 26, wherein said first signal path comprises another selector which during a normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during test operation supplies said test input signal to said signal input terminal of said circuit block.

29. The semiconductor device according to claim 26, wherein said second signal path comprises another selector which during a normal operation supplies a

normal clock to said clock input terminal of said circuit block, and which during a test operation supplies said test clock to said clock input terminal of said circuit block.

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30. The semiconductor device according to claim 26, wherein said selector selects a prescribed signal other than said test output signal and said test clock, and supplies the prescribed signal to said third pad during a normal operation.

31. A semiconductor device having an access time validity test mode, comprising:

a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;

a first signal path for guiding a test input signal, which has been supplied to a first pad, to a signal input terminal of said circuit block;

a second signal path for guiding a test clock, which has been supplied to a second pad, to a clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad via a dummy latch; and

a fourth signal path for guiding said test output signal, which has been output from said signal output terminal of said circuit block, to a fourth pad,

wherein said dummy latch is constituted so as to latch said test output signal at substantially a same operating speed as an operational latch for latching an output signal of said circuit block during a normal operation, and

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Cont. wherein said third signal path is formed so that a wiring delay time from said signal output terminal of said circuit block to said dummy latch is substantially equal to a wiring delay time from said signal output terminal of said circuit block to said operational latch.

32. The semiconductor device according to claim 31, wherein said first signal path comprises a selector which during the normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during a test operation supplies said test input signal to said input terminal of said circuit block.

33. The semiconductor device according to claim 31, wherein said second signal path comprises a selector which during the normal operation supplies a normal clock to said clock input terminal of said circuit block, and which during a test operation supplies said test clock to said clock input terminal of said circuit block.

34. The semiconductor device according to claim 31, wherein said third signal path comprises a selector which during the normal operation supplies a prescribed

signal other than said test output signal to said third pad, and which during a test operation supplies said test output signal to said third pad.

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35. The semiconductor device according to claim 31, wherein said fourth signal path comprises a selector which during the normal operation supplies a prescribed signal other than said test clock to said fourth pad, and which during a test operation supplies said test output signal to said fourth pad.

36. A semiconductor device having a setup time measuring test mode, comprising:

a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;

a first signal path for guiding a test input signal, which has been supplied to a first pad, to a signal input terminal of said circuit block;

a second signal path for guiding a test clock, which has been supplied to a second pad, to a clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad; and

a fourth signal path for selectively guiding said test clock input to said clock input terminal of said circuit block, and said test input signal input to said signal input terminal of said circuit block, as an output of the semiconductor device.

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37. The semiconductor device according to claim 36, wherein said fourth signal path comprises a selector which selectively supplies said test input signal or said test clock to a fourth pad.

38. The semiconductor device according to claim 36, wherein said fourth signal path is formed so that a wiring delay time when said test input signal is provided as the output of the semiconductor device is substantially equal to a wiring delay time when said test clock is provided as the output of the semiconductor device.

39. The semiconductor device according to claim 36, wherein said first signal path comprises a selector which during a normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during a test operation supplies said test input signal to said signal input terminal of said circuit block.

40. The semiconductor device according to claim 36, wherein said second signal path comprises a selector which during a normal operation supplies a normal

clock to said clock input terminal of said circuit block, and which during a test operation supplies said test clock to said clock input terminal of said circuit block.

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41. The semiconductor device according to claim 36, wherein said third signal path comprises a selector which during a normal operation supplies a prescribed signal other than said test output signal to said third pad, and which during a test operation supplies said test output signal to said third pad.

42. The semiconductor device according to claim 37, wherein said selector supplies a prescribed signal other than said test input signal and said test clock to said fourth pad during a normal operation.--
